

# CAN with flexible data-rate

Florian Hartwich

**Author**  
Florian Hartwich  
Robert Bosch GmbH  
P. O. Box 1342  
DE-72703 Reutlingen

**Link**  
www.bosch.com

Ever increasing bandwidth requirements in automotive networks impede the applicability of CAN due to its bit-rate limitation to 1 Mbit/s. To close the gap between CAN and other protocols, we have improved CAN in two ways:

- I Support of bit-rates higher than 1 Mbit/s,
- II Support of payloads larger than 8 byte.

We achieve this with a new frame format where we can switch inside the frame to a faster bit-rate for I and use a different data length cod-

ing for II. This new protocol is called "CAN with Flexible Data-Rate" or CAN-FD. CAN-FD protocol controllers are also able to perform standard CAN communication. This allows using CAN-FD in specific operation modes, e.g. soft-

## The CAN-FD frame format

The Control Field in normal CAN (ISO 11898-1) frames contains reserved bits, which are specified to be transmitted dominantly. In the CAN-FD frame, the reserved bit after the IDE bit (11-bit Identifier) or after the RTR bit (29-bit Identifier) is defined as Extended Data Length (EDL) bit and is transmitted recessively. This sets the receiving BSP and BTL FSMs into CAN-FD decoding mode.

The following bits are new in CAN-FD compared with CAN:

- ♦ EDL Extended Data Length
- ♦ r1, r0 reserved (transmitted dominantly)
- ♦ BRS Bit Rate Switch
- ♦ ESI Error State Indicator

The DLC values from 0000b to 1000b still code a Data Field length from 0 to 8 byte, while the DLC values from 1001b to 1111b are defined in CAN-FD to code Data Fields with a length of 12, 16, 20, 24, 32, 48, respectively 64 byte.

The EDL bit distinguishes between the normal CAN frame format and the CAN-FD frame format. The value of the BRS bit decides, whether the bit-rate in the Data-Phase is the same as in the Arbitration-Phase (BRS dominant) or whether the pre-defined faster bit rate is used in the Data-Phase (BRS recessive).

In CAN-FD frames, the EDL bit is always recessive and followed by the dominant r0 bit. This provides an

edge for resynchronization before an optional bit-rate switch. The edge is also used to measure the transmitter's loop delay for the optional TDC.

In CAN-FD frames, the transmitter's error state is indicated by ESI, dominant for error active and recessive for error passive. This simplifies network management.

There are no CAN-FD remote frames, the bit at the position of the RTR bit in normal CAN frames is replaced by the dominant r1 bit. However, normal CAN remote frames may optionally be used in CAN-FD systems. Receivers ignore the actual values of the bits r1 and r0 in CAN-FD frames.

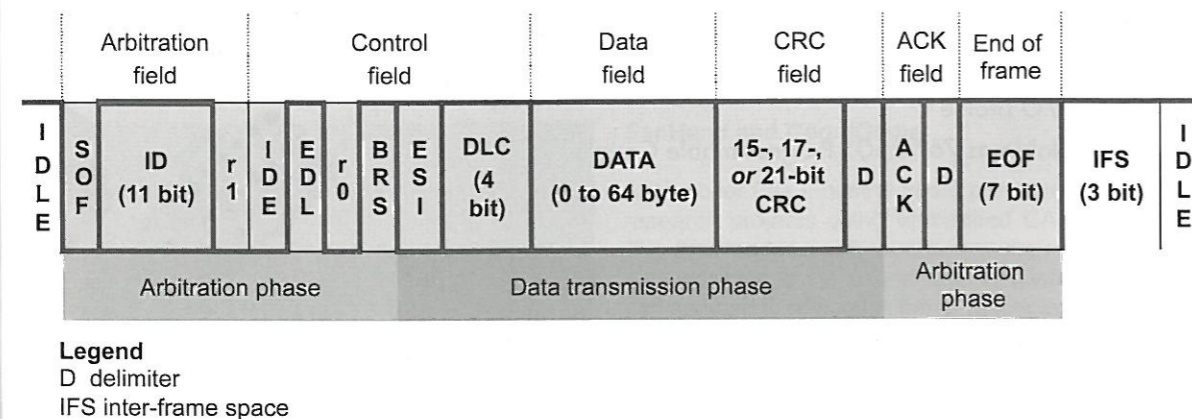


Figure 1: Format of the CAN-FD data frame with 11-bit identifier

ware-download at end-of-line programming, while other controllers that do not support CAN-FD are kept in standby.

The CAN-FD protocol [1] has been developed with the goal to increase the bandwidth of a CAN network while keeping unchanged most of the software and hardware (especially the physical layer). Consequently, only the CAN protocol controllers need to be enhanced with the CAN-FD option. The new frame format makes use of CAN's reserved bits. Via these bits, a node can distinguish between the frame formats during reception. CAN-FD protocol controllers can take part in normal CAN communication. This allows a gradual introduction of CAN-FD nodes into existing CAN systems.

## Basic principles

The CAN-FD protocol is a similar approach as proposed in [2] and [4] increasing the bandwidth by modification of the frame format. Two changes suggest themselves. Firstly, improving the header to payload ratio by allowing longer data fields. Secondly, speeding up the frames by shortening the bit time.

But these steps are only the groundwork, some additional measures are needed, e.g. to keep the Hamming distance of the longer frames at the same level as in normal CAN communication and to account for the CAN transmitter's loop delay.

The CRC polynomial of CAN is suited for patterns of up to 127 bit in length including the CRC sequence. Increasing the CAN frame's payload makes longer polynomials necessary.

In a CAN protocol controller, the Bit Timing Logic (BTL) state machine is evaluated once each time-quantum and synchronizes the position of the Sample-point to a specific phase in

relation to the edges in the monitored bit stream. Once each CAN bit-time, at the Sample-point, the bit-value is decided and the Bit Stream Processor (BSP) state machine is evaluated to decode (in transmitters to encode) the CAN frame. A shift register links the frame's serial bit stream with the controller's message memory.

CAN nodes synchronize on received edges from recessive-to-dominant on the CAN bus-line. The phases of their Sample-points are shifted relative to the phase of the transmitter's Sample-point. A node's specific phase-shift depends on the signal delay-time from the transmitter to that specific node.

The signal delay-time between the nodes needs to be considered when more than one node may transmit a dominant bit. This is the case in the arbitration field or in the acknowledge slot. The configuration of the CAN bit-time, especially the Propagation Segment's length and the Sample-point's position, must ensure that twice the maximum phase shift fits between the Synchronization Segment and the Sample-point. Once the arbitration is decided, until the end of the CRC Field, only one node transmits dominant bits, all other nodes synchronize themselves to this single transmitter. Therefore it is possible to switch to a pre-defined (shorter) bit-time in this part of a CAN frame, in CAN-FD called the Data-Phase. The rest of the frame, outside the Data-Phase, is called the Arbitration-Phase.

All nodes in the network must switch to this shorter bit-time synchronously at the start of the Data-Phase and back to the normal bit-time at the end of the Data-Phase. Figure 1 shows an example for the average bit-rate that can be achieved with a bit-rate of 0,5 Mbit/s in the Arbitration-Phase.

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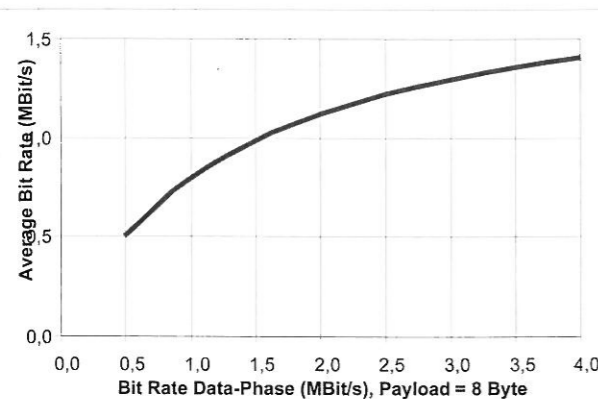


Figure 1: Speeding up from 0,5 Mbit/s to 4 Mbit/s

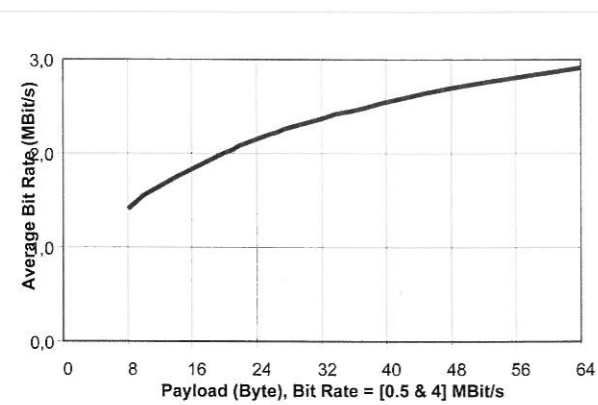


Figure 2: Enlarging a frame to 64 data bytes

tration-Phase and a higher bit-rate in the Data-Phase. In the example, an 11-bit identifier is used, and there are 8 data bytes in the frame. Stuff-bits are not considered. The example is extended in Figure 2: Lengthening the Data-Phase further increases the average bit-rate. The bit-rate is 0,5 Mbit/s in the Arbitration-Phase and 4 Mbit/s in the Data-Phase.

The factor between the short bit-time in the Data-Phase and the normal bit-time in the Arbitration-Phase decides how much the frames are speeded up. This factor has two limits. The first is the speed of the transceivers: Bits that are too short cannot be decoded. The second is the time-resolution of the CAN synchronization mechanism: after switching to the short bit-time, a phase error of one time quantum in the normal bit time needs to be compensated.

At the last bit of the Data-Phase, the CRC

Delimiter, all nodes switch back to the normal bit-time before the receivers send their acknowledge bit. Receivers are synchronized to the transmitter, but node-specific signal propagation times cause acknowledge bits of the most distant receivers to arrive after that of the nearest receivers. Therefore, a CAN-FD transmitter has to tolerate a 2-bit CRC Delimiter before the acknowledge bit. All CAN-FD nodes have to tolerate two consecutive dominant bits in the Acknowledge Slot. Latest, the second dominant Acknowledge Bit must be followed by a recessive Acknowledge Delimiter and the End-of-Frame field.

CAN's fault confinement strategy, where a node that detects an error in an ongoing frame immediately notifies all other nodes by destroying that frame with an error flag, requires that all nodes monitor their own transmitted bits to check for bit errors.

Current CAN transceivers may have, according to ISO 11898-5, a loop-delay (CAN-Tx pin to CAN-Rx pin) of up to 255 ns. In order to detect a bit error inside a bit-time of the Data-Phase, this bit-time has to be significantly longer than the loop-delay. To make the length of a short bit-time independent of the transceiver's loop delay, CAN-FD provides the Transceiver Delay Compensation (TDC) option.

### Additional CRC polynomials

The error detection capabilities and operational safety of the normal CAN protocol are discussed in [7], [8], and [9]. CAN-FD maintains all of CAN's fault confinement mechanisms, including Error Frames, error counters, error-active/passive modes, and positive acknowledging for fault-free messages. Since CAN-FD allows longer data fields than normal CAN, the CRC (Cyclic Redundancy Check) sequence needs to be adapted in order to keep the frame's Hamming Distance at the same value of 6. We chose two new BCH-type CRC polynomials: g17 for frames with up to 16 data bytes, g21 for frames with more than 16 data bytes.

$$g17 = x^{17} + x^{16} + x^{14} + x^{13} + x^{11} + x^6 + x^4 + x^3 + x^1 + 1$$

$$g21 = x^{21} + x^{20} + x^{13} + x^{11} + x^7 + x^4 + x^3 + 1$$

For this reason, the length of the CRC sequence in CAN-FD data frames depends on the DLC. At the beginning of a frame, all nodes, including the transmitter, start to calculate the frame's CRC sequence according to all three polynomials, g17, g21, and the normal CAN polynomial. When the frame format is decided in the Control Field and the DLC is transmitted, one of the three polynomials is selected. The transmitter uses the selected poly-

nomial to generate the frame's CRC sequence. The receivers use the applicable polynomial to decide whether the frame is to be acknowledged.

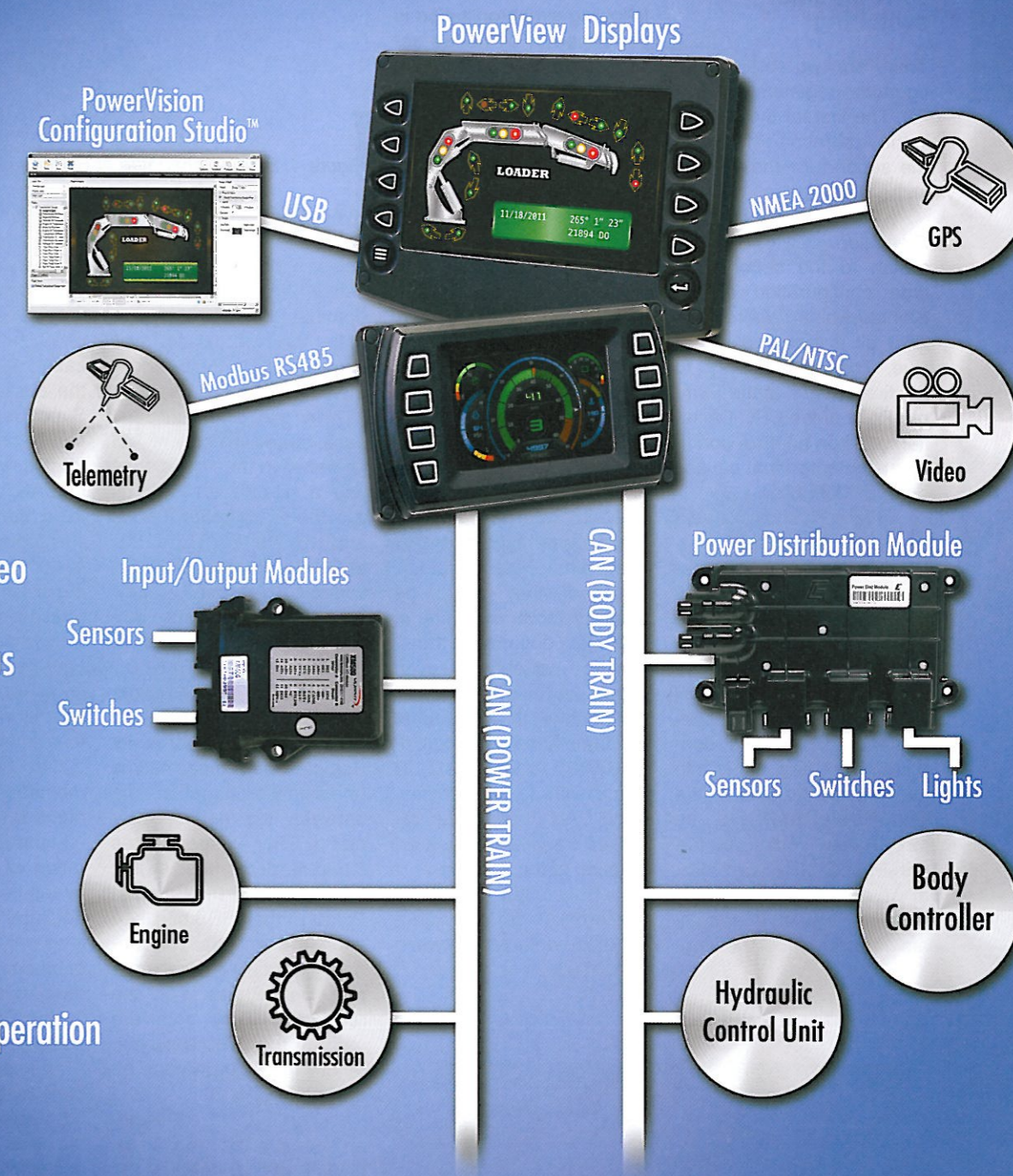
In normal CAN, the stuff-bits, which are inserted into the bit-stream to ensure that there are enough edges for resynchronization, are not considered for CRC calculation. As described e.g. in [7], two bit-errors may on rare occasion remain undetected when the first generates a bit-stuffing condition and the second then removes a stuff condition (or vice versa), shifting the position of the frame bits between the two bit-errors. The shifted area may lead to a burst error that is too long for the CRC mechanism.

The treatment of stuff-bits in CAN-FD is changed to ensure that this cannot happen. The simplest measure would have been to include all stuff-bits into the CRC calculation. However, this would prevent the well-proven CRC hardware implementation with the feedback shift-register that calculates the CRC sequence while the frame is in progress. The solution consists of two measures: Including the stuff-bits preceding the CRC sequence into the CRC calculation and changing the stuffing mechanism for the CRC sequence. Contrary to the normal CAN bit-stuffing method, where a stuff-bit of inverse polarity is inserted after every five consecutive bits of the same polarity, the positions of the stuff-bits in the CAN-FD's CRC sequence are fixed: The CRC sequence starts with a stuff-bit and additional stuff-bits are inserted after every four bits of the sequence. Each of these fixed stuff-bits has the inverse polarity of its preceding bit. The number of stuff-bits in the CRC sequence is equal to the maximum number of stuff-bits according to the normal CAN bit-

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stuffing mechanism. As in the normal CAN bit-stuffing mechanism, the maximum number of consecutive bits with the same value is five, the maximum distance between edges for resynchronization is ten.

### CAN bit-time switching

There are two sets of configuration registers in CAN-FD: The first for the bit-time in the Arbitration-Phase and the second for the bit-time in the Data-Phase.

The BTL and Bit-Rate Prescaler (BRP) FSMs switch to the second bit-time configuration at the Sample-Point where the BRS bit is sampled recessive. They switch back to the first bit-time at the Sample-Point of the CRC Delimiter, or when an error condition is detected that causes an error frame.

Figure 3 shows an example for the bit-time configurations, in which the data-rate in the Data-Phase is four times faster than in the Arbitration-Phase. Both, the length of  $t_q$  and the number of  $t_q$  in the bit-time may be different in the two configurations. The two configurations may be identical, but the bit-time in the Data-Phase may not be longer than in the Arbitration-Phase. The two bits, in which the bit-rate switch happens are of intermediate length, since the con-

figurations are switched at Sample-Points (see Figure 4). Together the two bits are as long as the sum of one of each of the bit-times.

Switching the bit-time configurations at the Sample-Point instead of after the end of Phase\_Seg2 is necessary to ensure that a following synchronization is performed in all nodes according to the parameters of the second bit-time configuration. Phase-shifts between the nodes may result in not all of them agreeing on the border between Phase\_Seg2 and the subsequent Sync\_Seg.

Figure 5 shows the simulation of a test case, in which CAN\_0 and CAN\_1 arbitrate for the CAN network. The signals CAN\_Tx and CAN\_Rx are the interface between the protocol controllers and the transceivers. The Sample-Point shows where the CAN-Rx input is captured. The signals  $f_{tx}$  and  $f_{rx}$  show where the bit-rate is switched; they could be used for mode switching in CAN-FD optimized transceivers, enabling even higher bit-rates in the Data-Phase. Both nodes send the same base CAN identifier. CAN\_0 sends a CAN-FD frame with 11-bit identifier, while CAN\_1 sends an extended frame and loses arbitration at the SRR bit.

Transmitters do not synchronize on "late" edges (those detected between

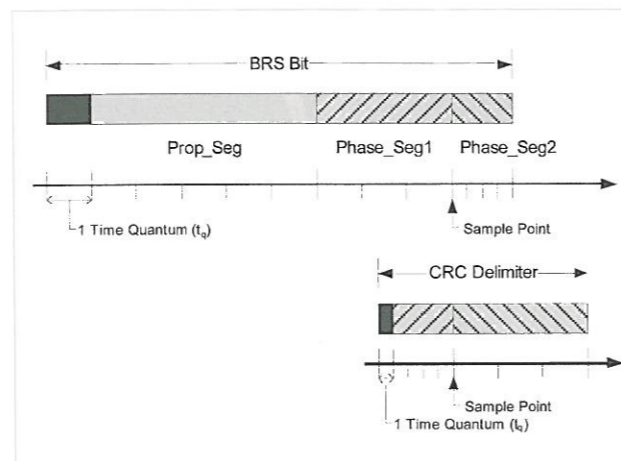


Figure 4: Bit-time changing at BRS bit and CRC Delimiter

Sync\_Seg and Sample-point) otherwise the transceiver loop-delay would cause them to lengthen dominant bits. So as transmitter, CAN\_1 did not synchronize on CAN\_0 before the edge from EDL to r0.

In the simulated test case, there is a delay of 433 ns between the nodes; they use a bit-rate of 1 Mbit/s in the Arbitration-Phase and 10 Mbit/s in the Data-Phase. At the SRR bit, where CAN\_1 loses arbitration, its Sample-Point is 350 ns (see strobes 1 and 2) earlier than that of CAN\_0.

CAN\_1 synchronizes to CAN\_0 at the edge from EDL to r0. Afterwards its Sample-Point comes 433 ns (the signal propagation time between the nodes) after that of CAN\_0 (see strobes 3 and 4). Both nodes switch their bit-rate at the Sample-Points of their BRS bits (see strobes 5 and 6). The signal  $f_{tx}$  shows the transmitter's Data-Phase,  $f_{rx}$  the receiver's. They both are reset at the CRC Delimiter, before the Acknowledge bit is sent by CAN\_1.

The CRC Delimiter seen by the transmitter CAN\_0 is prolonged by the signal propagation time, the Acknowledge bit conforms to the Arbitration-Phase's bit-rate.

The analog input signal at CAN\_Rx needs to be synchronized to the clock of the BTL FSM. Together with the BTL's time step size of one  $t_q$ , this digitization

delay limits the time resolution of the CAN bit-synchronization. This means a phase-error of up to one  $t_q$  may remain after a (re-)synchronization; the synchronization quality depends on the duration of the  $t_q$ . The Sync\_Seg with a fixed duration of one  $t_q$  compensates for this residual phase-error in CAN bit-timing, but one  $t_q$  in the first bit-time may correspond to several  $t_q$  in the second bit-time. The maximum possible residual phase-error has to be taken into account for the configuration. Setting  $t_q$  to the same duration in both configurations maximizes the tolerance range.

In existing CAN implementations, the maximum number of time quanta in a bit-time is 25, while the duration of the  $t_q$  is defined by the controller's clock period and the BRP. This allows only few combinations of bit-time configurations for the Arbitration-Phase and for the Data-Phase with the same  $t_q$  duration.

In automotive applications, with a bit-rate of e.g. 0.5 Mbit/s or 1 Mbit/s in the Arbitration-Phase, the acceleration in the Data-Phase is limited to a factor of about five. The reasons for this limit are the minimum pulse-width in the receive path of currently available transceivers and EMI considerations. In other applications, long bus-lines may limit the bit-rate in the Arbitration-Phase to e.g.

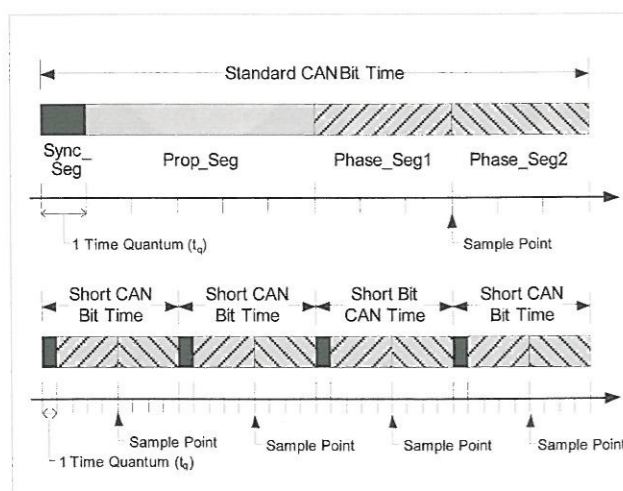


Figure 3: Normal and short CAN bit-times

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**Abstract**

This article describes the CAN-FD frame format with additional bits in the control field and the CRC sequences to secure longer frames with the same Hamming distance as in the existing CAN protocol. The configuration options for the two bit-rates are explained in detail. In addition, measurements of the upper limits for the bit-rate are discussed using the first hardware implementation of a CAN-FD protocol controller and off-the-shelf CAN transceivers chips.

125 kbit/s, enabling a higher acceleration factor.

Figure 6 shows how the average bit-rate of a CAN network that needs a bit-time of 8  $\mu$ s in Arbitration-Phase can be accelerated without exceeding the specification range of existing CAN transceivers in the Data-Phase. Figure 7 shows how this acceleration is increased when the Data field gets longer. The advantage of the improved header to pay-load ratio rises with the acceleration factor between Arbitration-Phase and Data-Phase.

ISO 11898-1 allows more than 8 tq for each of the bit-time segments Prop\_Seg, Phase\_Seg1, and

Phase\_Seg2. We increased the configuration range to 16 tq for Phase\_Seg2 and to 64 tq for the sum of Prop\_Seg and Phase\_Seg1 in our CAN-FD implementation. This allows a wide range of bit-time combinations with the same tq length. The range of the SJW (Synchronization Jump-Width) configuration is also increased to 16 tq for CAN-FD applications. This enables a high acceleration factor with a low residual phase-error at the BRS bit.

**Transceiver Delay Compensation**

Current CAN transceivers may have, according

to ISO 11898-5, a loop delay (from the CAN-Tx pin to the CAN-Rx pin) of up to 255 ns. Since transmitters are required to check for errors in their transmitted bits, this would set a lower limit for the bit time in the Data-Phase if the check needs to be done at the bit's Sample-point.

Measurements have shown that existing CAN transceivers are able to transmit and receive bits that are shorter than their loop-delay. In this case the check for bit-errors needs to be delayed until the bit value, which is transmitted at the CAN-Tx output is looped-back to the CAN-Rx input. This is the purpose

**CAN-FD measurements**

The development of the CAN-FD protocol went in parallel with the design of CAN-FD protocol controllers for simulative verification and for laboratory evaluation. Main topics of the analysis were the new protocol features and the limits set by the physical layer. The measurements were based on FPGA implementations of CAN-FD and a multi-node CAN network with off-the-shelf CAN transceivers (e.g. NXP TJA1040). For the measurements shown here, the network consists of seven nodes connected by a linear bus-line topology. The distance between the terminations at node T2 and node R9 is 42 m, the bit-rate switches from an Arbitration-Phase at 0,5 Mbit/s to Data-Phases at 12 Mbit/s or at 15 Mbit/s.

It is not expected a bit-rate of 15 Mbit/s can be reached in automotive conditions with existing transceivers. The examples intend to show that the bit-rate in the Data-Phase is not limited by the signal propagation-time in the transceivers and on the CAN bus-lines.

Special attention was given to the effects of the transceiver loop-delay (see Figure I). In this example, the transceiver's loop-delay is 126 ns at room temperature. This is almost twice the Data-Phase's bit time, here 66,67 ns at 15 Mbit/s.

The output pin T2\_Tx already starts the DLC before the ESI bit reaches the input pin T2\_Rx or, after the bus-line delays, the receivers' input pins R3\_Rx and R9\_Rx.

The example in Figure II shows a complete CAN-FD frame with 29-bit CAN-identifier and 64 data bytes.

Here the complete Data-Phase is (at 12 Mbit/s) shorter than 23 bit of the Arbitration-Phase. In the example, there is CAN arbitration in the first bits of the CAN identifier, superposition of Acknowledge bits from near and from distant receivers virtually prolongs that bit.

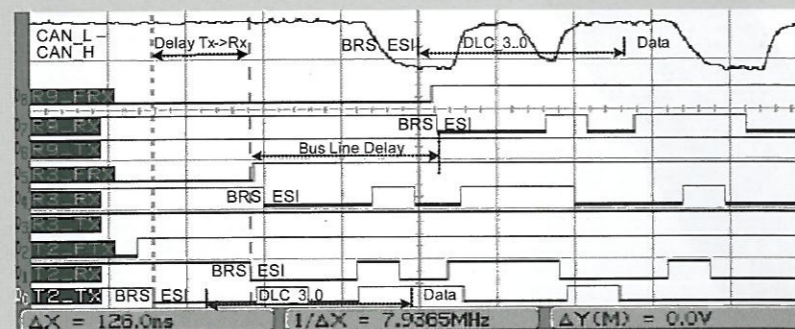


Figure I: CAN-FD Transceiver loop delay

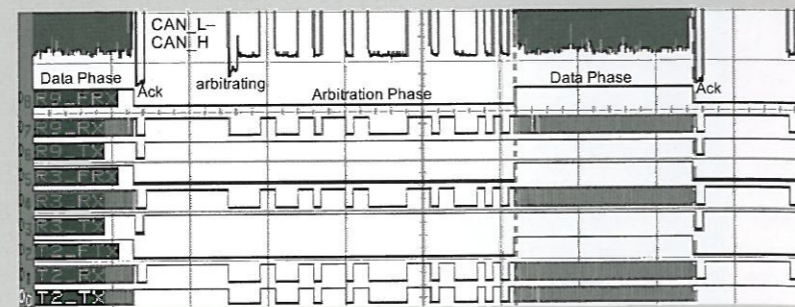


Figure II: CAN-FD frame with 64 data bytes and 12 Mbit/s in the data-phase

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### Conclusion

CAN-FD is a new protocol that combines CAN's core features with a higher data-rate. For automotive applications using star-topologies, CAN-FD targets an average data rate of 2,5 Mbit/s with existing CAN transceivers, resulting in the same effective payload as a low-speed Flexray network.

Using bus-line topologies will allow data-rates up to 8 Mbit/s. There is an easy migration path from CAN systems to CAN-FD systems since CAN application software can be left unchanged (apart from configuration). The Bosch CAN IP modules are currently being adapted to optionally support the CAN-FD protocol.

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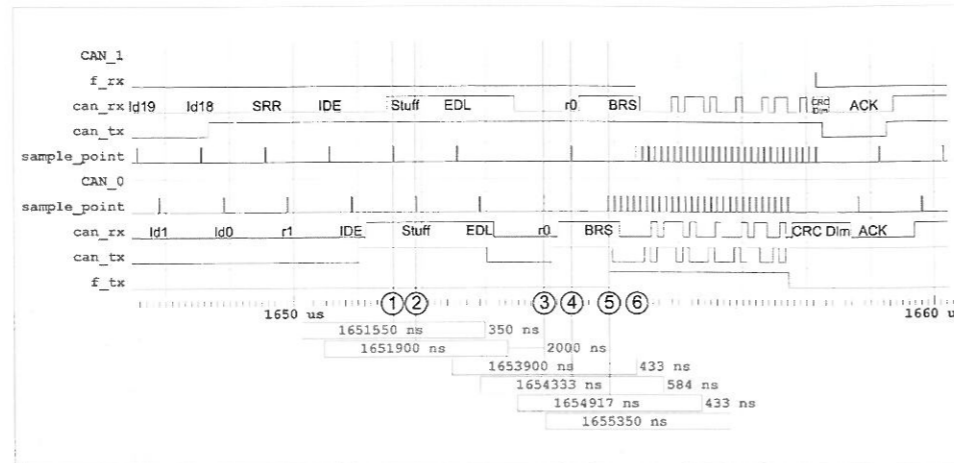


Figure 5: CAN-FD bit-time switching after bus arbitration

of the optional TDC mechanism of CAN-FD. Receivers do not need this mechanism. Transmitters apply it in the Data-Phase of a frame.

The point-in-time where the looped-back bit-value is checked is named the Secondary Sample Point (SSP). The actual loop-delay is not a static value; it depends apart from silicon parameters mainly on the operating temperature.

The CAN-FD protocol controller is able to perform a delay measurement to find the optimum position for the SSP. Within each CAN-FD frame, the transmitter measures the delay between the data transmitted at the CAN-Tx output and the data received at the CAN-Rx input. The measurement is performed when the arbitration is decided, but before the bit-rate is switched at the edge from EDL-to-r0. The delay is measured (in system clock periods) by a counter that starts at the beginning of the r0 bit at CAN-Tx and stops when the edge is seen at CAN-Rx (see Figure 8).

The result is a node-specific value. It does not depend on signal propagation-times on the CAN bus-line. A configurable offset is added to the measured delay-value to place the SSP into the middle of the bits seen at CAN-Rx.

When the TDC mechanism is enabled, it changes the way how a transmitter

checks for bit-errors during the Data-Phase of a CAN-FD frame from direct comparison of transmitted and received bits at the CAN Sample-Point to a delayed comparison at the SSP.

The position of the SSP is always relative to the start of a transmitted bit. It may be more than one bit-time after the end of that bit. Transmitted bits are buffered until the SSP is reached. Then their value is compared with the

actual value of the input signal to check for bit-errors. If a bit-error is detected, this information is buffered until the next CAN Sample-Point is reached, where it is presented to the BSP FSM. The BSP FSM answers to the bit-error according to the rules of the CAN fault confinement with a CAN Error frame; the bit-rate is switched back to that of the Arbitration-Phase. When no bit-error is detected until the Sample-

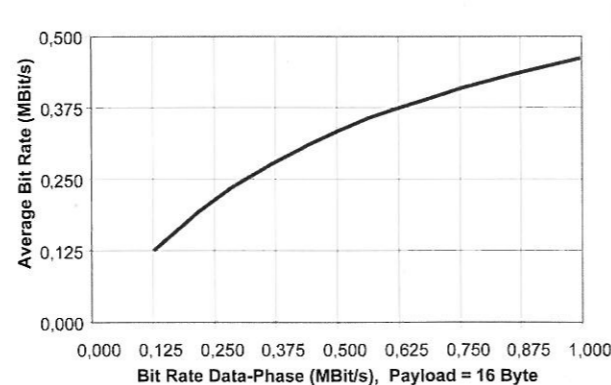


Figure 6: CAN-FD example for long bus lines

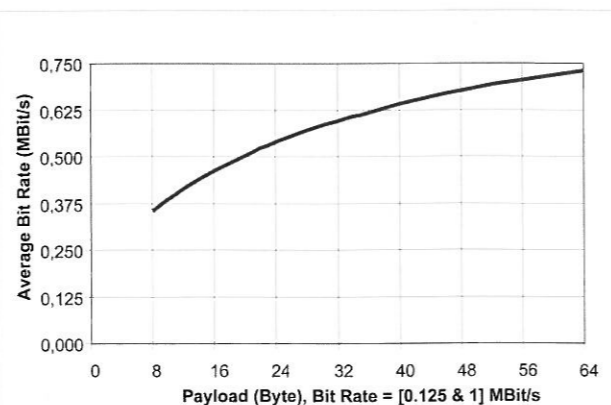


Figure 7: Average bit-rates for long bus lines

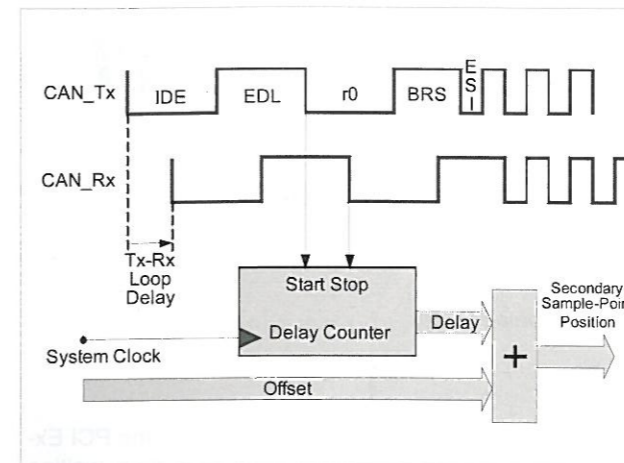


Figure 8: Measuring the transceiver loop delay

Point of the CRC Delimiter is reached, the CAN-FD protocol controller switches back the bit-rate and returns to normal bit-error checking. The transmitters disregard the actual value of the CRC Delimiter bit using the TDC mechanism. A global error at the end of the CRC field will cause the receivers to send error frames that the transmitter will detect during Acknowledge or End-of-Frame (EOF).

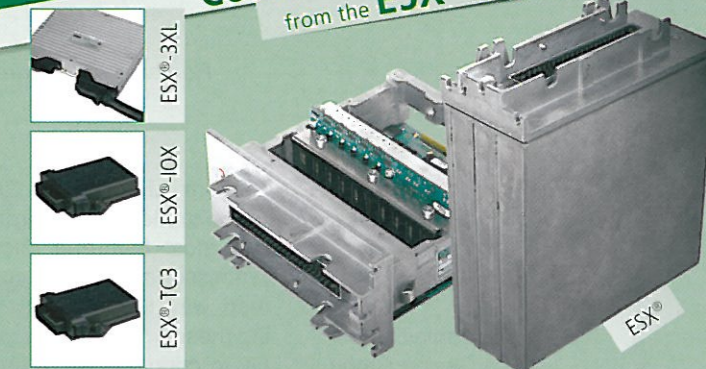
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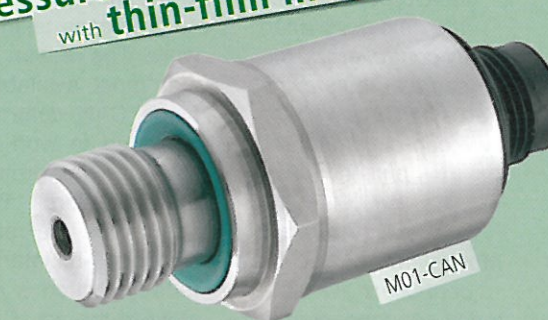
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Sensor-Technik Wiedemann GmbH  
Am Bärenwald 6 · 87600 Kaufbeuren  
Germany  
Telephone +49 (0)83 41-95 05-0